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MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE--ETC(U)
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MANUFACTURING METHODS AND TECHNOLOGY REPORT

CONTRACT DAAB07-C-0041

MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This First Quarterly Report for Contract DAAB07-76-C-0041 describes the progress and status of this program to establish cost-effective production capability for Miniature High Voltage Multiplier Modules for use in power supplies.
A brief description of the PERT Chart is given and the initial design work on capacitors, rectifiers and substrates, is described.

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FIRST QUARTERLY REPORT

MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

CONTRACT NO. DAAB07-76-C-0041

PERIOD COVERED: 12 JULY, 1976 TO 30 SEPTEMBER, 1976

PREPARED BY: A. KENNEDY

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ABSTRACT

This First Quarterly Report describes the rectangular and curved miniature high voltage multiplier modules for use in low cost power supplies for second generation image intensifier tubes. General approach is to set up cost-effective production capability, utilizing already established component technologies and materials and to demonstrate the pilot line capability to fabricate devices at the rate of 125 acceptable units per 40 hour week.

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PURPOSE

This Contract covers component designs, mounting and interconnection techniques, tooling and test methods and other manufacturing methods and techniques required for production of rectangular and curved miniature high voltage multiplier modules. These units are to be used in low cost power supplies for second generation image intensifier tubes. The full scope and details of the specification are given in SCS-495, Appendix A.

The Thermometer Chart Figure 1 shows the program task and target completion dates from start to finish of the project. Major milestones consist of delivery of (1) first and second engineering samples and test data, (2) production line layout and schedule, (3) confirmatory samples and test data, (4) production line set-up, (5) pilot production run, (6) production rate demonstration, (7) preparation and publication of a final report.

The general approach to the component is to design and set-up a cost-effective production capability, utilizing already established device technologies and materials, and to demonstrate the production line capability to fabricate at the rate of 125 acceptable units per 40 hour week.

THERMOMETER CHART - TARGET COMPLETION DATES

DATE		DAYS	
		720	
21 May/78	23	690 ...	FINAL REPORT
		....	7TH QUARTERLY REPORT
21 Apr/78	22	660 ...	PILOT RUN SAMPLES & REPORT
		....	NARRATIVE REPORT - MONTHLY
22 Mar/78	21	630 ...	PRELIMINARY PILOT RUN & REPORT
		....	NARRATIVE REPORT - MONTHLY
20 Feb/78	20	600	
		....	NARRATIVE REPORT - MONTHLY
21 Jan/77	19	570 ...	6TH QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
22 Dec/77	18	540 ...	CONFIRMATORY SAMPLES & REPORT
		....	NARRATIVE REPORT - MONTHLY
22 Nov/77	17	510	
		....	NARRATIVE REPORT - MONTHLY
23 Oct/77	16	480 ...	5TH QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
23 Sep/77	15	450	
		....	NARRATIVE REPORT - MONTHLY
24 Aug/77	14	420	
		....	NARRATIVE REPORT - MONTHLY
25 Jul/77	13	390 ...	4TH QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
25 Jun/77	12	360 ...	2ND ENG. SAMPLE & REPORT
		....	NARRATIVE REPORT - MONTHLY
26 May/77	11	330	
		....	NARRATIVE REPORT - MONTHLY
26 Apr/77	10	300 ...	3RD QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
27 Mar/77	9	270	
		....	NARRATIVE REPORT - MONTHLY
25 Feb/77	8	240	
		....	NARRATIVE REPORT - MONTHLY
26 Jan/77	7	210 ...	2ND QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
27 Dec/76	6	180 ...	1ST ENG. SAMPLE & REPORT
		....	NARRATIVE REPORT - MONTHLY
27 Nov/76	5	150	
		....	NARRATIVE REPORT - MONTHLY
28 Oct/76	4	120 ...	1ST QUARTERLY REPORT
		....	NARRATIVE REPORT - MONTHLY
28 Sep/76	3	90	
		....	NARRATIVE REPORT - MONTHLY
29 Aug/76	2	60	
		....	NARRATIVE REPORT - MONTHLY
30 Jul/76	1	30 ...	PERT CHART TO BE SUBMITTED
12 Jul/76	0	0	
DATE		DAYS	

FIG. 1.

SECTION 1

1.1 DESIGN APPROACH

This section reviews the design approach and manufacturing process which will be used in the production of rectangular and curved miniature high voltage multiplier modules. The process flow chart listing each major process step is shown in Fig. 9. Because there are only geometrical differences between the curved and rectangular multiplier modules, a single process outline will be sufficient.

1.2 THE VOLTAGE MULTIPLIER

A high voltage power supply for low current applications can best be achieved by the use of cascading multiplier stages. A basic "N" stage multiplier circuit is shown in Fig. 2.

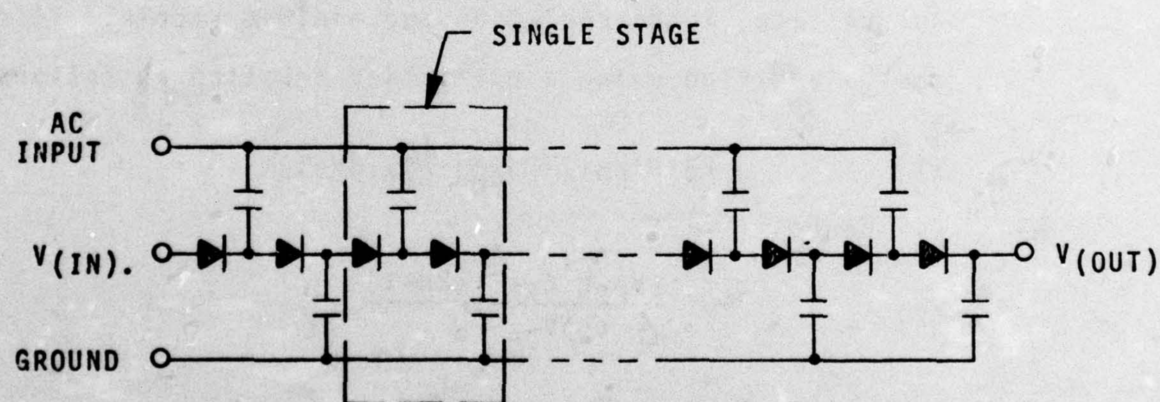


FIG. 2. "N" STAGE MULTIPLIER CIRCUIT

The construction of such a circuit uses discrete diodes and capacitors simply connected to develop a d.c. output that is a multiple of the peak-to-peak input voltage. Almost any voltage can be achieved by increasing multiplier stages. The voltage is limited only by the ratings of the components and materials used.

An ideal voltage multiplier characteristic is not easily achieved in practice and it is commonly observed that load regulation of multiplier circuits rapidly degrades as the multiplication is increased. Factors such as ripple, frequency and capacitance values play an important role in multiplier design and performance.

Experience in the design of Second Generation power supplies has shown that capacitor values of approximately 50pF, per stage, are necessary to give the necessary output voltage, load regulation and minimum ripple. This can be verified using a multiplier equation as follows:

(1) $$E_o = NV_{pp}\left(1-2N\frac{C_s}{C_m}\right) - \frac{I_L}{C_m f}(2N-1)$$

hence

(2) $$C_m = \frac{2V_{pp}N^2 C_s + \frac{I_L}{f}(2N-1)}{NV_{pp}-E_o}$$

where

C_M = multiplier capacitance

I_L = load current

f = frequency

N = number of double stages

C_S = rectifier capacitance

V_{PP} = peak-to-peak input voltage

E_O = output voltage

to find C_M and assuming that

N = 6

f = 25KHz

I_L = 500nA

C_S = 0.2pF

E_O = 5700 volts

V_{PP} = 1000 volts

the

C_M = 48.7pF

The above equations apply to ideal conditions, In reality the stray or fringing capacitance plays a significant role and must be considered and designed into the overall capacitor value requirements.

1.3 MULTIPLIER CONSTRUCTION

In general multipliers are assembled using discrete diodes and capacitors. Considerable multiplier size reduction has been achieved using discrete diodes and

ceramic parallel or series bank capacitors. The manufacturing techniques are simple but labor intensive and consequently expensive. The use of discrete diodes makes further miniaturization impossible beyond certain limits.

The objective of this program is to develop miniature, low cost high voltage multiplier modules for use in low cost power supplies for second generation intensifier tubes. Because the stress is on miniaturization and low cost it was decided to adopt already existing technologies within the corporate structure, mainly that of high voltage diodes and high voltage ceramic capacitor. Since both products will not be considered as part of the development program it will be possible to optimize production techniques to manufacture the specified multiplier modules from readily available components.

The design and fabrication of voltage multipliers will be realized by the use of custom designed/parallel capacitor banks and silicon high voltage rectifier pellets.

The multipliers will use two (2) 0.040 inch thick six section parallel ceramic capacitor banks. This thickness is considered to be the optimum for the K-1200 material and volts/mil rating.

A. CURVED CAPACITOR BANKS

An electrode pattern has been designed for the curved multiplier in such a way that when any two (2) capacitor banks are sandwiched, the rectifier chips can be placed between the capacitor plates to form a voltage multiplier. Each capacitor bank, illustrated in Fig. 3 by drawing No. TSK-25-249, will have six (6) plates with sufficient area to provide the necessary multiplier capacitance. This slanted electrode pattern allows diode pairs to be placed on each pad, providing the characteristic series string of diodes of the parallel multiplier.

B. RECTANGULAR CAPACITOR BANKS

The same basic approach as outlined for the curved multiplier will be used for the oblong multiplier. Two (2) 0.040 inch thick rectangular ceramic blocks will be sandwiched with rectifier chips between them. However, constricted package size necessitates dissimilar electrode patterns on opposing ceramic capacitor banks to achieve the interconnecting diode configuration. This is illustrated in Fig. 4 and Fig. 5 by drawings TSK-25-247 and TSK-25-248.

C. DIODE SUBSTRATE

It is proposed that a tooled ceramic or similar type of material, forms a substrate in which are located diode pellets at their exact position within the multiplier electrode pad configuration. This substrate is illustrated in Fig. 6 drawing number TSK-313-100 for the curved multiplier and in Fig. 7 drawing number TSK-312-100 for the rectangular multiplier. The already pre-tested diodes will be inserted into the substrate locating holes and then sealed within the substrate using thermosetting epoxy resin. The diode leads will then be trimmed and both faces of the substrate lapped to expose the silver lead terminations of the diode pellets. The lapped diode substrate assembly will be tested to ensure that device parameters did not alter during the lapping/cleaning operation. The multiplier input and output leads will be located in the substrate grooves near the input and output diodes. The assembly will be inserted between the two opposing capacitor banks. Interconnection between the diodes and the capacitors will be made using silver conducting epoxy. For assembly illustration see Fig. 8, drawing No. TSK-312-102 and for Process Flow Chart see Fig. 9.

SECTION 2.

STATUS AND FUTURE WORK

This section describes the status of work against the various tasks outlined in Figure 1.

2.1 PERT

A PERT Chart covering the entire program was prepared and submitted 9/6/76. This plan has been accepted.

2.2 THE CAPACITOR DESIGN

On 19 August 1976 a meeting was held with the capacitor manufacturer (Erie Technological Products, 644 West 12th Street, Erie, PA) to discuss the capacitor design, manufacture feasibility and delivery time of the prototype samples.

During the discussion it became evident that the rectangular capacitor electrode pads, contained within such a small area would produce high stray and parasitic capacitance values that would equal or even exceed the required calculated values of approximately 30 pF per capacitor. To reduce the stray capacitance it became necessary to reduce the electrode pad area leaving only sufficient area for electrical connections. The most promising electrode pad configuration was of the "dumb-bell" design (see Fig. 10). Since the manufacture of

this type of electrode presented no major technological problems, a prototype sample of rectangular banks was ordered for initial trials. A delivery time of four (4) to five (5) weeks was promised by the manufacturer.

2.3 THE SUBSTRATE EVALUATION

A small sample of substrate was manufactured to the originally proposed design. The material used was glass filled epoxy and the main purpose was to evaluate the feasibility of the design.

The rectifier pellets were encapsulated in the substrate with thermo-setting epoxy. The excess diode leads were trimmed and the substrates lapped, by hand, on 400 grade carborundum paper. The following problem areas were identified:

(a) The diode body length between devices varied up to 0.015 inches making accurate diode location in the substrate impossible;

(b) because of the diode body length variations accurate substrate lapping was impossible;

(c) the diode location within the substrate required very complex jigging arrangement;

(d) difficulty in making good input/output lead connections to the diodes and the substrate.

2.4 THE DIODES

Both the single and double junction diodes are in the process of being manufactured for evaluation purposes. No problems or delays are anticipated.

2.5 CAPACITOR SAMPLE MECHANICAL INSPECTION

The ordered capacitor samples were received on 27th Sept 1976. For dimensional evaluation see Table 1. For capacitor pads dimensional values see Table 2.

2.6 CAPACITOR ELECTRICAL TESTS

Samples of capacitors are undergoing capacitance value tests and breakdown strength tests, but final results were not available at the time of publication.

2.7 SUBSTRATE DESIGN CHANGE PROPOSALS

(a) The diode body length variations are inherent in the process and little can be done to control the accuracy.

To overcome this problem it is proposed to increase the substrate thickness to a level where diode length variations will become less significant in the substrate design.

(b) To ensure a more positive and accurate diode location as well as simplify the diode jigging arrangements the substrate design was modified as shown in Fig. 11. A sample of the new design is being manufactured and the assemblies will be evaluated.

SECTION 3.

CONCLUSIONS

In the initial effort on this program it was possible to establish capacitor pad design that would reduce stray capacitance. Manufacture of prototype substrates assemblies demonstrated the unsuitability of the originally proposed design regarding diode pellet assembly and complexity of jigging required in the assembly operation. New substrate design is proposed and will be evaluated. All effort is on the rectangular multiplier and once the major problem areas are identified and resolved, evaluation of the curved multiplier components will proceed.

SECTION 4.

PROGRAM FOR NEXT QUARTER

During the next quarter, electrical capacitor parameters will be evaluated and prototype multipliers built. Multiplier efficiency and breakdown characteristics measured. The new substrate design will be evaluated and alternative substrate materials investigated.

SECTION 5.

PUBLICATION AND REPORTS

No reports or publications were made on the work associated with this program during the current quarter.

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
DIMENSIONS IN INCHES—DO NOT SCALE THIS DWG.

BTSK-25-249

ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (pF) ±TOL./SECT.
6.0 KV DC	+25°C	20 pF ± 20%

1.2 TEMPERATURE CHARACTERISTIC (X5R)

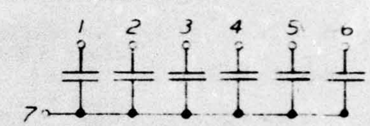
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 KV AT 25°C.

1.4 INSULATION RESISTANCE AT TEST VOLTAGE (+25°C) 100 KM OR 1000MΩ μF.

1.5 CAPACITANCE AT 25°C, 1KHz, 1VRMS AND WORKING VOLTAGE - (SEE TABLE ABOVE).

1.6 D.F. UNDER SAME CONDITION AS REF 1.5 SHOULD BE <2.5%

1.7 SCHEMATIC



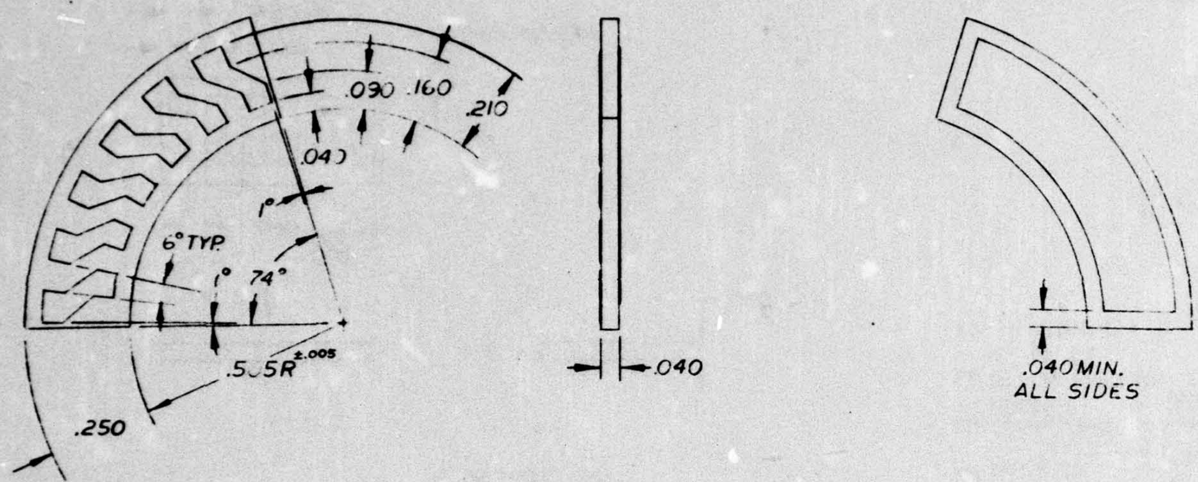


FIG. 3.

SCALE: 4=1

PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS	± —
DECIMAL	±.002
ANGLES	±0°30'

DWN. K. CRAM MAR.8/76 CKD.

MATERIAL

BTSK-25-249 REV.

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
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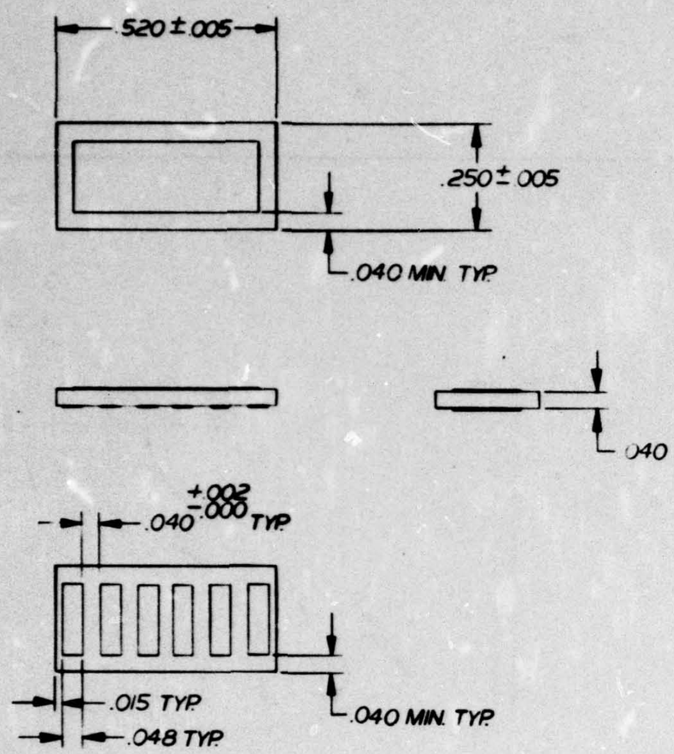


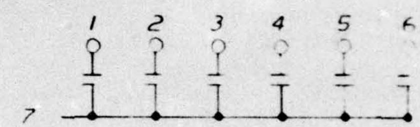
FIG. 4.

ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (P.F.) & TOL. / SECT.
6.0 K.V.	+ 25°C	20PFD ± 20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.
1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 KM. OR 1000 M.Ω MFD.
1.5 CAPACITANCE AT 25°C. & 1KHZ., 1V. R.M.S. & WORKING VOLTAGE. — SEE TABLE ABOVE.
1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.
1.7 SCHEMATIC



SCALE:

ERIE TECHNOLOGICAL PRODUCTS

PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS	± ——
DECIMAL	± .002
ANGLES	± 0°30'

DWN. CHK. MATERIAL

BTSK-25-247 REV.

DIMENSIONS IN INCHES—DO NOT SCALE THIS DWG.

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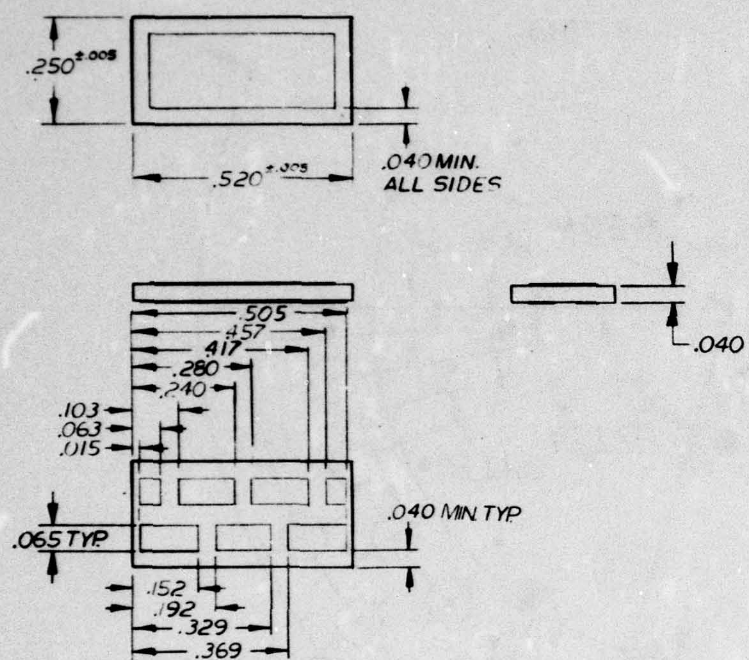


FIG. 5.

ELECTRICAL SPECIFICATION

1.1

WORKING VOLTAGE	OPERATING TEMPERATURE	CAP. (PF.) & TOL. / SECT.
6.0 K.V.	+ 25°C	20PFD ±20%

1.2 TEMPERATURE CHARACTERISTICS (X5R)

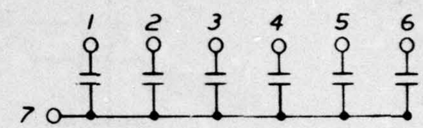
1.3 DIELECTRIC STRENGTH TEST VOLTAGE 9.0 K.V. AT 25°C.

1.4 INSULATION RESISTANCE AT TEST VOLTAGE + 25°C. — 100 KM. OR 1000 M.Ω MFD.

1.5 CAPACITANCE AT 25°C. & 1KHZ., 1V. R.M.S. & WORKING VOLTAGE. — SEE TABLE ABOVE.

1.6 D.F. UNDER SAME CONDITION AS REF. 1.5 SHOULD BE < 2.5%.

1.7 SCHEMATIC



SCALE: 4=1

[redacted]

ERIE

PARALLEL BANK CAPACITOR

TOLERANCES UNLESS OTHERWISE SPECIFIED		DWN. L. MACKLIN MAR/9/76	CKD.
FRACTIONS	± —	MATERIAL	
DECIMAL	± .002	BTSK-25-248	REV.
ANGLES	± 0°30'		

BTSK-25-248

REV.

APPROVED

ATSK-313-100

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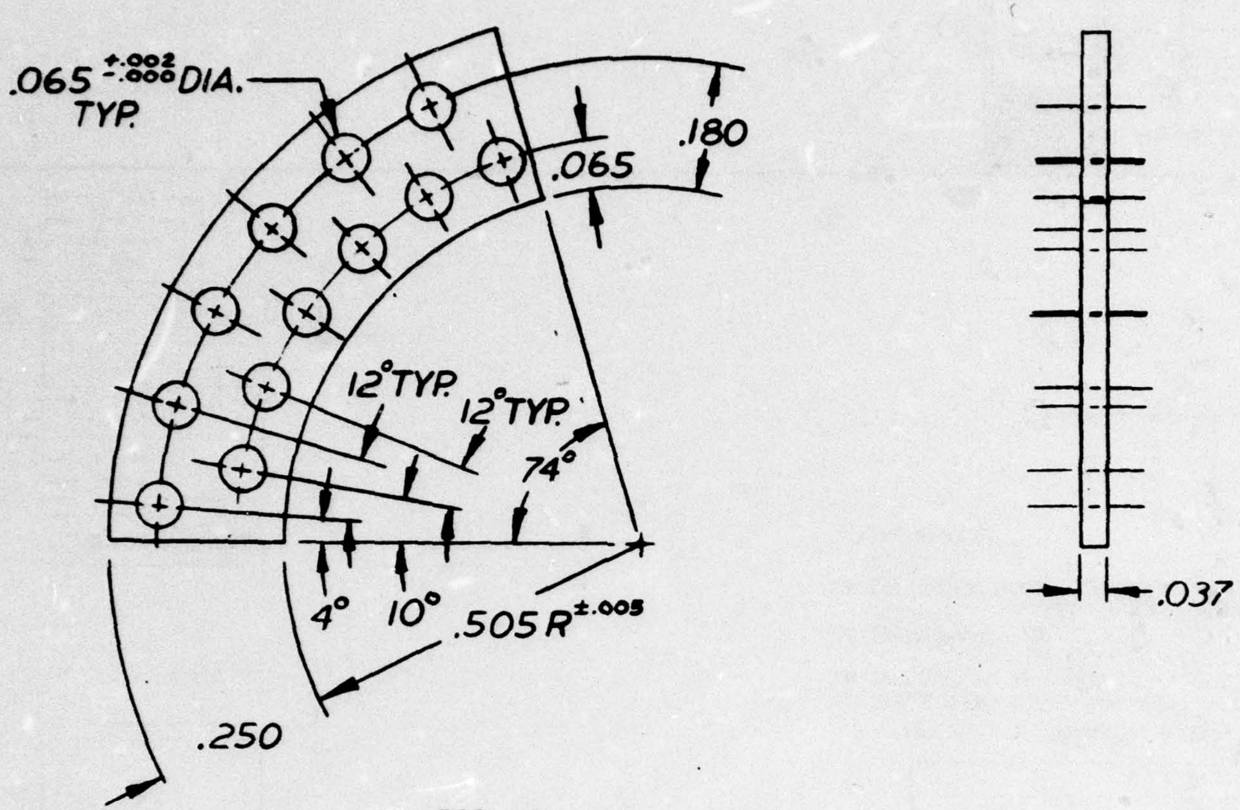


FIG. 6

SCALE: 4=1

ERIE TECHNOLOGICAL PRODUCTS INC

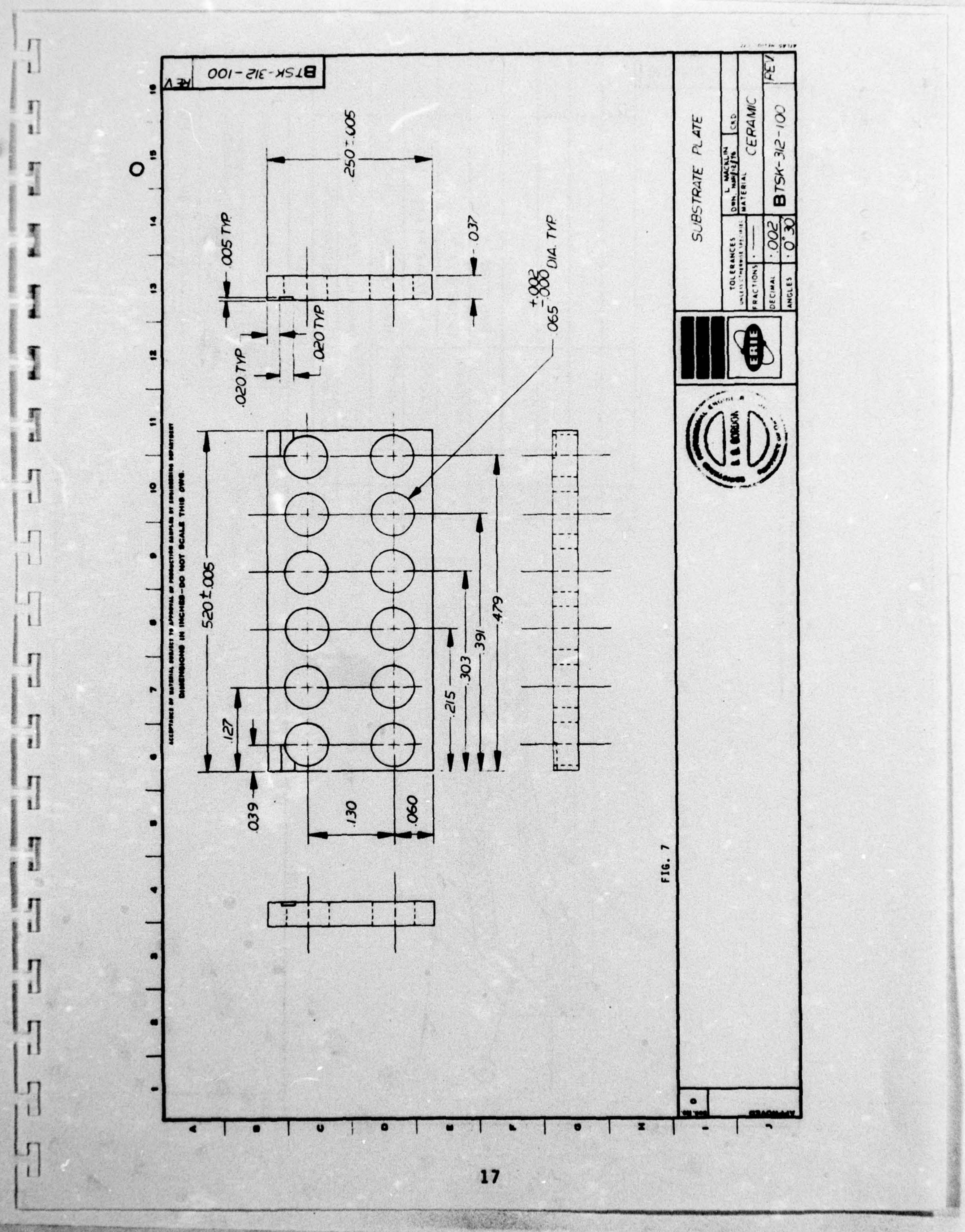
REGISTERED PROFESSIONAL ENGINEER B. E. GORDON PROVINCE OF ONTARIO

SUBSTRATE PLATE

TOLERANCES UNLESS OTHERWISE SPECIFIED		DWN. K. CRAM MAR. 12/76	CKD.
FRACTIONS	± —	MATERIAL CERAMIC	
DECIMAL	± .002		REV.
ANGLES	± 0°30'	ATSK-313-100	

SUB. NO. 0

APPROVED



BTSK-312-100
REV
ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
DIMENSIONS IN INCHES—DO NOT SCALE THIS DWG.
.005 TYP
.250±.005
.037
.020 TYP
.020 TYP
$.065^{+.002}_{-.000}$ DIA. TYP
.520±.005
.127
.039
.215
.303
.391
.479
.130
.060
SUBSTRATE PLATE
TOLERANCES
FRACTIONS
DECIMAL .002
ANGLES 0°30'
L. MACKLIN
MATERIAL
CERAMIC
BTSK-312-100
ERIE

FIG. 7

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
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BTSK-312-102

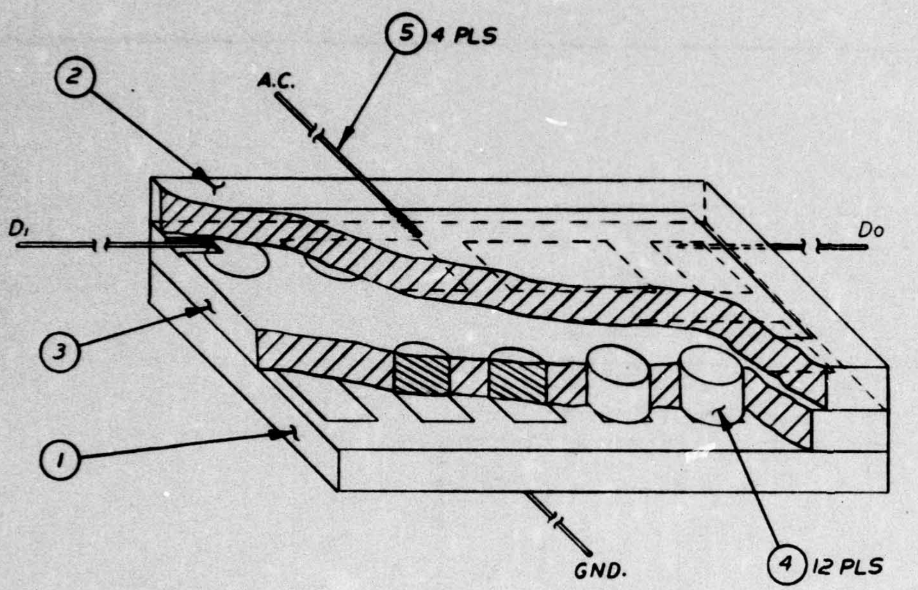


FIG. 8

REF.	QTY.	PART NO.	DESCRIPTION	MFG.
9				
8				
7				
6				
5	4	——	BUS WIRE	——
4	12	ATSK-312-101 REV. —	DIODE ASS'Y	ERIE
3	1	BTSK-312-100 REV. —	SUBSTRATE PLATE	ERIE
2	1	BTSK-25-248 REV. —	PARALLEL BANK CAPACITOR	ERIE
1	1	BTSK-25-247 REV. —	PARALLEL BANK CAPACITOR	ERIE

PARTS LIST

MULTIPLIER ASSEMBLY

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± ——
DECIMAL ± ——
ANGLES ± ——

DWN. K. CRAM MAR 12/76 CKD.
MATERIAL

BTSK-312-102 REV.

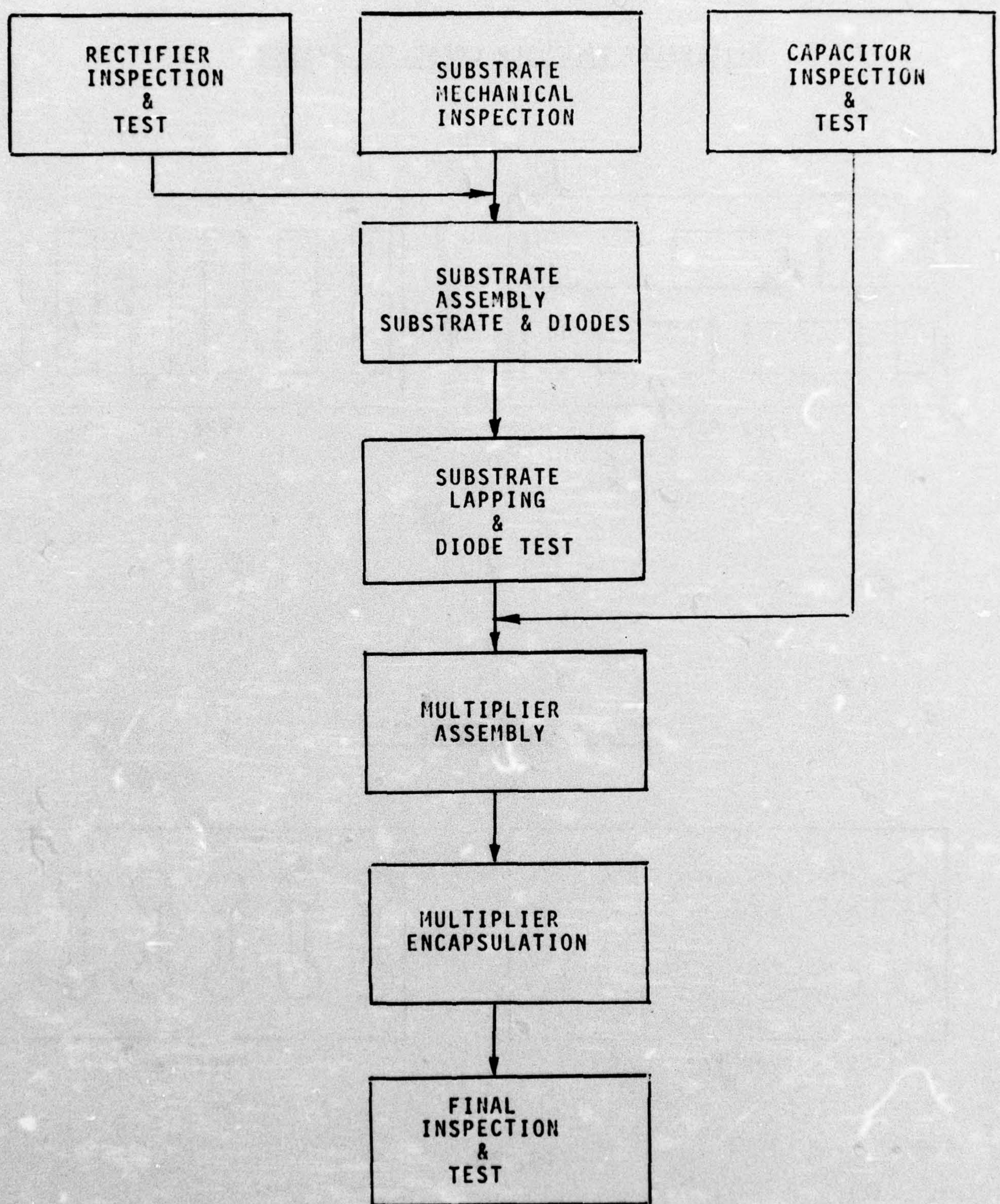
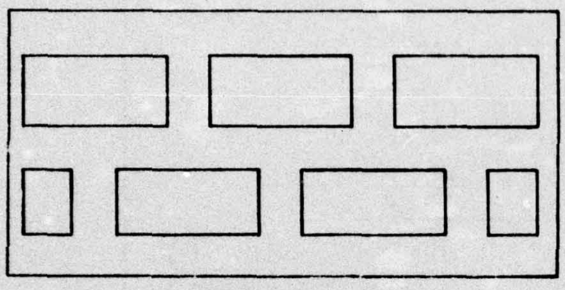
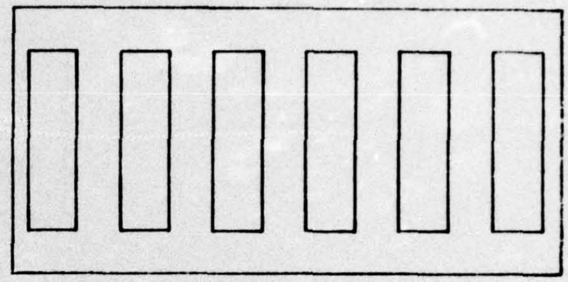


FIG. 9 PROCESS FLOW CHART

ORIGINALLY PROPOSED CAPACITOR DESIGN

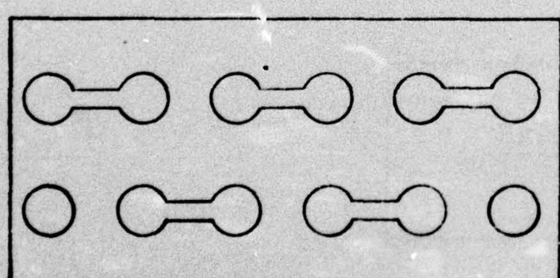


TYPE "A"

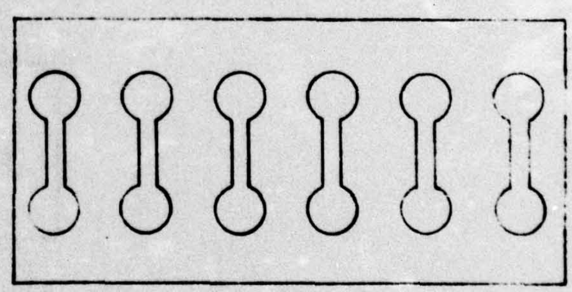


TYPE "B"

RE-DESIGNED CAPACITOR



TYPE "A"



TYPE "B"

FIG. 10.

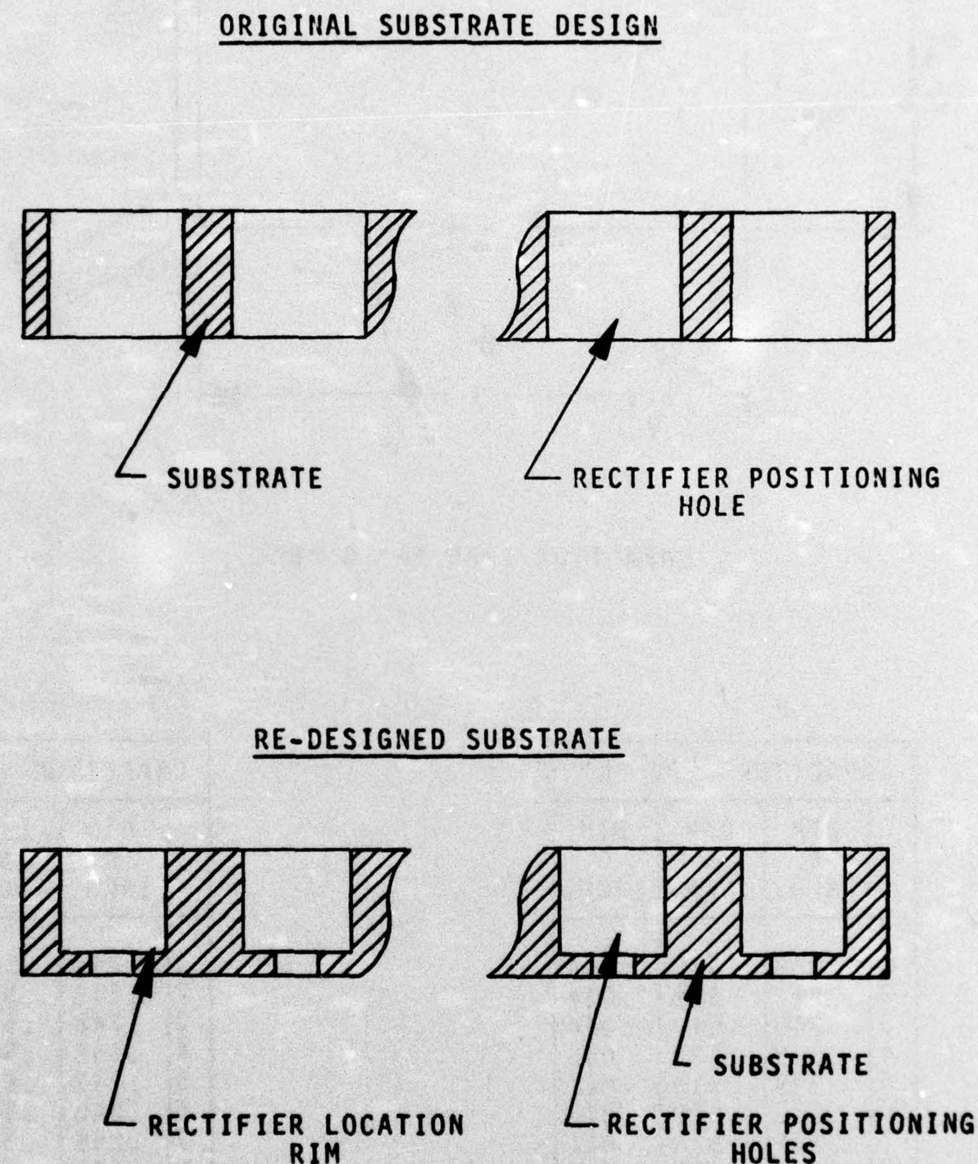
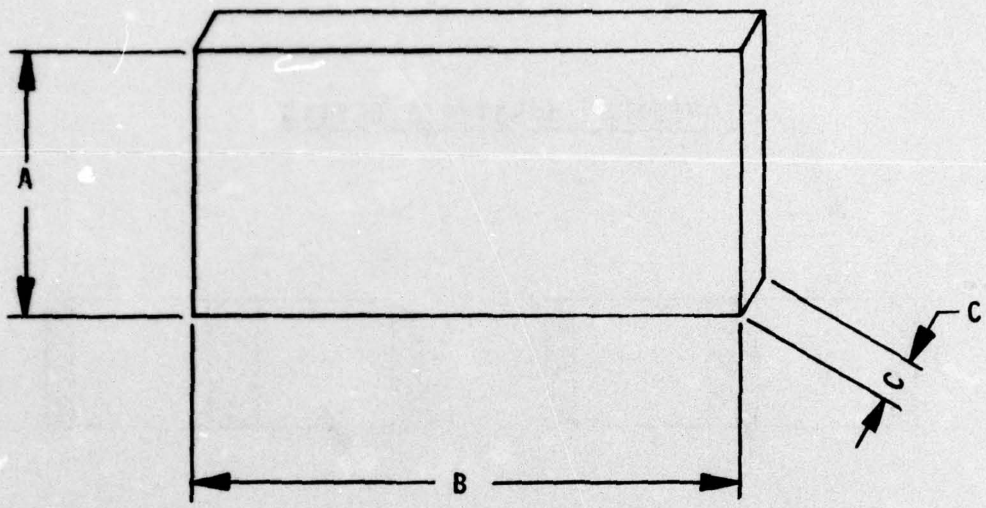

ORIGINAL SUBSTRATE DESIGN
SUBSTRATE
RECTIFIER POSITIONING HOLE
RE-DESIGNED SUBSTRATE
SUBSTRATE
RECTIFIER LOCATION RIM
RECTIFIER POSITIONING HOLES

FIG. 11.

CAPACITOR MECHANICAL INSPECTION



CAPACITOR TYPE "A" & "B"

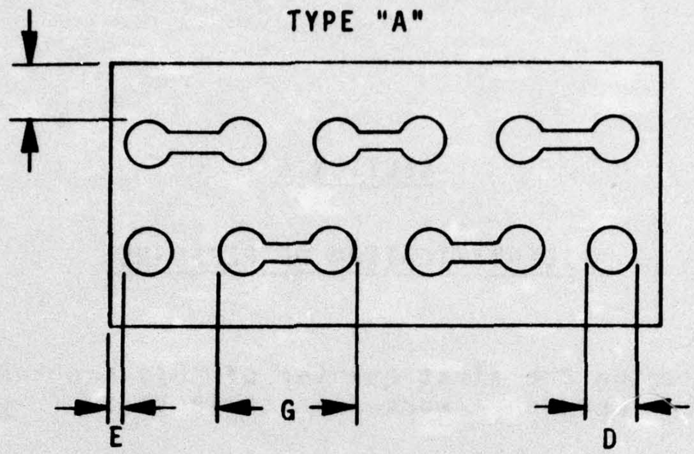
CAPACITOR TYPE "A"	DIM A INCH.	DIM B INCH.	DIM C INCH.
1	.248	.518	.044
2	.247	.519	.044
3	.249	.519	.044
4	.249	.523	.045
5	.248	.519	.042
6	.248	.520	.044
7	.249	.520	.044
8	.249	.512	.043
9	.247	.512	.044
10	.247	.518	.045
11	.245	.515	.045
12	.247	.519	.042

CAPACITOR TYPE "B"	DIM A INCH.	DIM B INCH.	DIM C INCH.
1	.246	.515	.044
2	.248	.515	.043
3	.248	.516	.044
4	.248	.521	.043
5	.247	.513	.045
6	.248	.519	.043
7	.246	.512	.043
8	.247	.519	.045
9	.249	.520	.043
10	.247	.516	.042
11	.246	.516	.043
12	.248	.516	.044

TABLE I

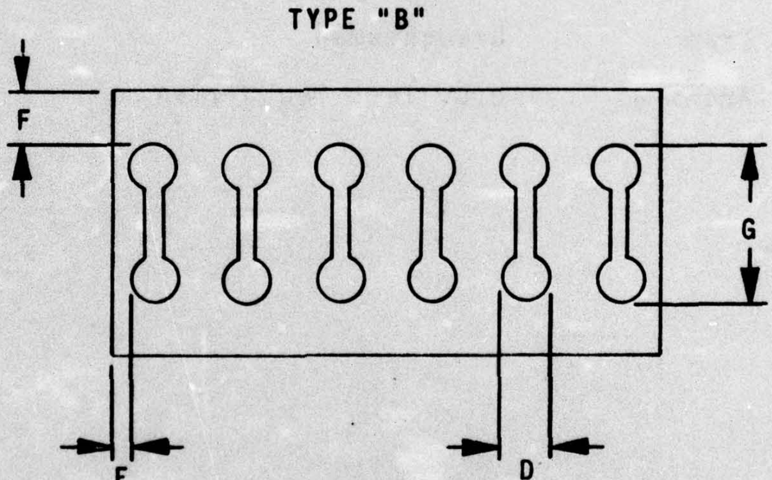
CAPACITOR PAD MECHANICAL INSPECTION

TYPE "A"



	DIMENSION D			DIMENSION E			DIMENSION F			G
	MIN.	MAX.	AVE.	MIN.	MAX.	AVE.	MIN.	MAX.	AVE.	AVE.
1	.0319	.0468	.0413	.0129	.0273	.0182	.0339	.0407	.0372	.145
2	.0404	.0449	.0430	.0122	.0187	.0160	.0318	.0377	.0342	.149
3	.0428	.0449	.0442	.0130	.0182	.0161	.0326	.0399	.0368	.146
4	.0362	.0472	.0450	.0137	.0213	.0172	.0308	.0405	.0359	.150

TYPE "B"



	DIMENSION D			DIMENSION E			DIMENSION F			DIM G
	MIN.	MAX.	AVE.	MIN.	MAX.	AVE.	MIN.	MAX.	AVE.	AVE.
1	.0401	.0530	.0439	.0112	.0192	.0156	.0290	.0385	.0346	.182
2	.0384	.0439	.0413	.0089	.0193	.0144	.0321	.0402	.0366	.186
3	.0416	.0452	.0437	.0075	.0216	.0150	.0282	.0406	.0350	.186
4	.0408	.0440	.0424	.0090	.0200	.0145	.0296	.0404	.0350	.184

TABLE II

SECTION 6

IDENTIFICATION OF PERSONNEL

During the first quarter of this program the following personnel worked in their area of responsibility:

INDIVIDUAL	RESPONSIBILITY	HRS. SPENT
P. Ransom	General Manager-High Voltage Products	50
A. Kennedy	Program Manager	212
G. Gordon	Senior Electronic Engineer	33
D. Platt	Manager, Quality Assurance & Control	24
V. Glenn	Q.A. Assistant	19
K. Cram	Draughtsman	38
D. Archard	Q.C. Test Technician	16

A. KENNEDY: Manager Semiconductor Engineering

PROGRAM RESPONSIBILITY: Program Manager

CURRENT ASSIGNMENT

Mr. Kennedy is responsible for research and development of silicon high voltage devices for military, industrial and commercial applications. These devices have ratings in the range 1000 to 50,000 volts per device, and 5 to 1000mA.

He has been responsible for the development of miniature silicon rectifiers specifically for use in voltage multipliers and power supplies for Gen I and Gen II night vision systems.

Of particular relevance to this program is the recent development of controlled avalanche devices with extremely low reverse leakage currents, typically less than 2 nanoamps at 2000 volts.

Other assignments at this time are the development of a controlled avalanche rectifier, (15KV) for the T.V. tripler application having fast turn-on and turn-off characteristics, and a 10KV rectifier for use in microwave ovens.

A miniature rectifier for Gen I power supplies developed by Mr. Kennedy's group is currently in production at the rate of approximately 10,000 per week.

ACADEMIC & PROFESSIONAL BACKGROUND

H.N.C. (Higher National Certificate) in Applied Physics, North Staffordshire College of Technology, England.

1969 - 1974 Production Manager, International Rectifier Company, Northern Ireland.

1963 - 1969 Senior Process Engineer, International Rectifier Company, England.

1956 - 1963 Development Engineer, Semiconductors, Nelson Research Laboratories, English Electric Company, England.

G. GORDON   Senior Electronic Engineer

PROGRAM RESPONSIBILITY

Electrical design of the voltage multiplier, including rectifier and capacitor characteristics and ratings. Assessment and analysis of performance data, with particular reference to its suitability for use in Gen II power supplies.

CURRENT ASSIGNMENTS

Mr. Gordon is in charge of an engineering development group engaged in the development of power supplies for Gen I and Gen II night vision applications. Recently he was responsible for the development and manufacture of prototype "single" oscillator power supplies for 18 and 25mm Gen II systems.

Is also working on state-of-the-art designs for miniature power supplies for CRT, laser and infra-red applications.

ACADEMIC & PROFESSIONAL BACKGROUND

BA. Sc. Electrical Engineering, University of Toronto.
Member of the Association of Professional Engineers of Ontario.
1971 to present, Development Engineer with Erie Technological Products Canada, Limited.

D. PLATT Manager, Quality Assurance & Control

PROGRAM RESPONSIBILITY - Quality Engineer, in charge of the Qualification Testing Program, and Quality Requirements.

CURRENT ASSIGNMENTS

In his capacity as Manager of Q.A. & Q.C., for the High Voltage Division of Erie Technological Products Canada, Limited, Mr. Platt is in charge of all Q.A., Q.C., process control, testing and inspection functions. The Erie Q.A., system is approved to U.S. and Canadian MIL standards.

ACADEMIC & PROFESSIONAL BACKGROUND

1974	Executive Seminar - Quality Assurance.
1972	Metrology, Loyalist College, Ontario.
1970-1971	Statistical Methods in Quality Control, Quality Control Management.
1969-1970	Solder certification course, U.S. Army Work Simplification. Mathematics.
1968-1969	Statistical Quality Control. Introduction to Quality Control.
1968	3 - year course in Electronics and T.V. Servicing,DeVry Institute of Technology.
1968 to present	Employed by Erie Technological Products of Canada, Ltd.

B. HEIDT Senior Technologist

PROGRAM RESPONSIBILITY

Test and evaluation of voltage multipliers with particular reference to their suitability for use in Gen II power supplies.

CURRENT ASSIGNMENT

Mr. Heidt is responsible for the circuit design, packaging and evaluation of prototype Gen II power supplies, 18 & 25mm types. Developed the master-slave and the single oscillator concepts. Has worked in this area since 1971.

ACADEMIC & PROFESSIONAL BACKGROUND

Honour graduate Electronic Major, Quinte Secondary, Ontario.
Honour graduate Engineering Technologist, Northern Institute of Technology, Toronto.
Member of OACETT.

1971 to present	Senior Technologist with Erie Technological Products of Canada, Ltd.
1969-1971	Maintenance Technician, Hitchon Radio Ltd.
1967-1969	Lecturer in Electronics Radio College of Canada, Toronto.

P. MAPLES Senior Engineering Technician

PROGRAM RESPONSIBILITY

Packaging Voltage Multipliers.

CURRENT ASSIGNMENT

Is responsible for mechanical packaging and assembly of a variety of high voltage power supplies, including miniature types to MIL specifications for night vision, infra red, photomultiplier, etc., applications. Is qualified as a certified instructor on soldering (U.S. Army course).

ACADEMIC & PROFESSIONAL BACKGROUND

Completed two years of O.N.C., course in England.
Member, Institute of Printed Circuits.
Certified Instructor on Soldering U.S. Army.
Course on Business Organisation, Loyalist College, Ontario.
Government Training course, Instrument Maker.

1939-1941	Evening course in Engineering.
1972 to present	Employed as Senior Engineering Technician by Erie Technological Products of Canada, Ltd.
1964-1972	Technical Specialist, Northern Electric Ltd.
1961-1964	Manager of Prototype and Test Dept., I.T.T., England.
1941-1951	Instrument Maker, Aron Electrical Motors Ltd., England.

F. TREVERTON   Senior Test Technician

PROGRAM RESPONSIBILITY

Designing and building special test equipment and fixtures necessary.

CURRENT ASSIGNMENT

Responsible for the design and assembly of special test equipment and fixturing used in the testing of high voltage power supplies and voltage multipliers, particularly for Gen I and Gen II night vision power supplies. Also carries out special tests and responsible for production testing of high voltage systems.

ACADEMIC & PROFESSIONAL BACKGROUND

1971	Electronic Technician Diploma, Loyalist College, Ontario.
	Chairman of Student Branch I.E.E.E. Member of Analog/Hybrid Computer Educational Society.
1971 to present	Employed by Erie Technological Products of Canada, Ltd., as Test Technician.

APPENDIX A

MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

1. SCOPE

1.1 This specification covers the requirements for miniature high voltage hybrid multiplier modules for use in low cost power supplies for second generation image intensifier tubes.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATIONS

Military

MIL-P-11268	Parts, Maintenance, and Processing used in Electronic Equipment

STANDARDS

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-109	Quality Assurance Terms and Definitions
MIL-STD-129	Marking for Shipment and Storage
MIL-STD-130	Identification Marking of U.S. Military Property
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-454	Standard General Requirements for Electronic Equipment
MIL-STD-456	Electronic Parts, Date and Source Coding for
MIL-STD-781	Reliability Test Exponential Distributions

3. REQUIREMENTS

3.1 Item definition. The miniature high voltage hybrid multiplier module, hereafter called the multiplier, shall be a solid state electronic device to convert a sinusoidal (AC) input voltage to a high DC output voltage. The multiplier shall consist of an "N" stage diode capacitor array connected in parallel.

3.1.1 The major components of the multiplier are the individual diode pellets and capacitor array.

3.2 Characteristics.

3.2.1 Room temperature performance. Unless otherwise stated, the multiplier shall meet the following minimum requirements at room temperature when operated from a 1000 volt peak to peak sine wave input over a frequency range of 20 KHz to 40 KHz.

3.2.1.1 Multiplier efficiency. The multiplier efficiency (6.3) shall be a minimum of 85% from no load (less than 2 nanoamps) to full load (500 nanoamps). (See 4.5.3.1).

3.2.1.2 Input capacitance. The input capacitance shall be less than eight (8) picofarads at 500 volts peak to peak. (See 4.5.3.2).

3.2.1.3 Charging current. The multiplier peak charging current at no load shall be less than one hundered-fifty (150) microamps. (See 4.5.3.3).

3.2.1.4 Ripple voltage. The multiplier ripple voltage shall be less than 3% peak to peak at no load. (See 4.5.3.4).

3.2.2 Physical characterisitics. The physical characteristics of the multiplier shall be as specified herein.

3.2.2.1 Resistance to soldering heat. The multiplier shall suffer no mechanical or electrical damage after its leads have been immersed in a solder bath at 450°F for at least 3 seconds. (See 4.5.6).

3.2.2.2 Solderability. Each multiplier lead shall be at least 95% covered with a solder coating when immersed in a solder bath, and any pinholes shall be concentrated in one area and do not exceed 5% of the total soldered area. (See 4.5.9).

3.2.2.3 Terminal strength. Each multiplier lead shall be capable of withstanding a 1/4 pound pull for a minimum of 5 seconds, with no rupturing of the lead or other damage to the lead or multiplier.

3.2.2.4 Dimensions. Dimensions shall be as specified in Figure 3. (See 4.5.2).

3.2.2.5 Weight. The weight of each multiplier shall not exceed 5 grams. (See 4.5.2).

3.2.3 Reliability (mean time to failure). The multiplier shall have a specified mean time to failure of 25,000 hours. There shall be no evidence of physical or electrical damages as indicated by an open circuit or short circuit. In addition the multiplier shall meet the following requirements:

a. Multiplier efficiency shall be as specified in 3.2.1.1.

b. Charging current shall be as specified in 3.2.1.3. (See 4.5.17)

3.2.4 Environmental conditions.

3.2.4.1 High temperature performance. Unless otherwise stated, the multiplier shall meet the following minimum requirements at high temperature plus 52°C when operated from a 1000 volt peak to peak sine wave input over a frequency range of 20 KHz to 40 KHz. (See 4.5.5).

3.2.4.1.1 Multiplier efficiency. The multiplier efficiency shall be a minimum of 80% from no load to full load and shall not change more than plus or minus 2% from its room temperature efficiency. (See 4.5.5.1).

3.2.4.1.2 Input capacitance. The input capacitance shall be less than eight (8) picofarads at 500 volts peak to peak.

3.2.4.1.3 Charging current. The multiplier peak changing current at no load shall be less than 300 microamps. (See 4.5.5.3).

3.2.4.1.4 Ripple voltage. The multiplier ripple voltage shall be less than 3% peak to peak at no load. (See 4.5.5.4).

3.2.4.2 Low temperature performance. Unless otherwise stated, the multiplier shall meet the following minimum requirements at minus 54 C when operated from a 1000 volt peak to peak sine wave input over a frequency range of 20 KHz to 40 KHz. (See 4.5.4).

3.2.4.2.1 Multiplier efficiency. The multiplier efficiency shall be a minimum of 80% from no load to full load and shall not change more than plus or minus 2% from its room temperature efficiency. (See 4.5.4.1).

3.2.4.2.2 Input capacitance. The input capacitance shall be less than eight (8) picofarads at 500 volts peak to peak. (See 4.5.4.2).

3.2.4.2.3 Charging current. The multiplier charging current at no load shall be less than 150 microamps.

3.2.5.2.4 Ripple voltage. The multiplier ripple voltage shall be less than 3% peak to peak at no load.

3.2.4.3 Environmental stress conditions.

3.2.4.3.1 Thermal shock. The multiplier shall show no evidence of mechanical or electrical damage when subjected to thermal shock. (See 4.5.13).

3.2.4.3.2 High Temperature Storage. There shall be no evidence of mechanical or electrical damage after the multiplier has been subjected to a minimum of 8 hours storage at plus 71°C. The multiplier shall be capable of meeting the requirements of 3.2.4.1.1 and 3.2.4.1.3 after it has been subjected to high temperature storage. (See 4.5.14).

3.2.4.3.3 Low temperature storage. There shall be no evidence of mechanical or electrical damage after the multiplier has been subjected to a minimum of two (2) hours storage at minus 65°C. The multiplier shall be capable of meeting the

requirements of 3.2.4.2.1 and 3.2.4.2.3 after it has been subjected to low temperature storage. (See 4.5.15).

3.2.4.3.4 Humidity sealing. There shall be no evidence of mechanical or electrical damage after the multiplier has been exposed to a relative humidity of not less than 95% at a temperature of not less than plus 23°C for a period of not less than six (6) hours. (See 4.5.16).

3.2.4.3.5 Mechanical shock. With the operating potential applied to the multiplier, there shall be no evidence of continuous arcing or breakdown, nor shall there be any abrupt changes in charging current when the multiplier is subjected to the following mechanical shock. Additionally, there shall be no evidence of mechanical damage. (See 4.5.12).

3.2.4.3.5.1 Longitudinal sawtooth. The multiplier shall withstand not less than ten (10) mechanical shock pulses along the transverse axis at an amplitude of 140 ±10 g's sawtooth wave peak for nine (9) millisecond ±10 percent duration.

3.2.4.3.5.2 Longitudinal impulse. The multiplier shall withstand not less than six (6) mechanical shock pulses along the longitudinal axis, in each direction, of not less than 500 g's half sine wave peak for 0.3 ±0.05 millisecond duration.

3.2.4.3.6 Mechanical vibration. With the operating potential applied to the multiplier, there shall be no evidence of continuous arcing or breakdown nor shall there be any abrupt changes in input current when the multiplier is subjected to

the followinq mechanical vibration: 2.5 g peak sine wave vibration over the frequency range of ten (10) Hertz through thirty-five hundred (3500) Hertz along both the longitudinal and transverse axis of the multiplier including three (3) five (5) minute dwells at the upper and lower frequency in each axis. (See 4.5.11).

3.2.4.3.7 Reduced Barometric Pressure. The multiplier shall show no evidence of continuous arcing or breakdown nor shall there be any abrupt changes in charging current after subjection to a barometric pressure of 3.44 inch for one hour. The multiplier shall show no evidence of mechnaical damage after subjection to a barometric pressure of 3.44 inch for one hour. (See 4.5.10).

3.3 Design and construction.

3.3.1 Materials, components, design and construction. Compatible materials, processes and techniques will be utilized for fabricating conductive and dielectric films in predetermined patterns and sequences to provide for the interconnection of diode pellets and capacitors to form a parallel array of cascaded doubler stages. There shall be no adverse physical interation between thick film components substrate, dielectric or attached active devices. Thick film elements will be considered as compatible only if they have been developed to the point of having all conductive dielectric insulating and passivating films constitute a system wherein no deleterious

metallurgical reactions between any one of the system components occurs as a result of any processing or operating sequence. The contractor is not limited in his choice of processes other than that each process used to fabricate the multiplier shall be mutually compatible with each other. The techniques utilized shall have been optimized and capable of being controlled so that the multiplier can be reproducibility and repetitively fabricated with operational, environmental and reliability characteristics equivalent to those requirements specified herein. (See 4.5.2.1).

3.3.1.1 Materials and components. Materials shall be as specified herein. Materials not specified shall be selected by the contractor and shall be subjected to all provisions of the specification with conformance to MIL-P-11268.

3.3.1.2 Terminals. (See 4.5.2.1)

3.3.1.2.1 Terminal type. Terminal type shall be as shown in Figure 3.

3.3.1.2.2 Terminal location and length. Location and length shall be as specified in Figure 3.

3.3.2 Identification and marking. The multiplier shall be marked in accordance with MIL-STD-130 with the type designation, the MS part number the manufacturer's name or code symbol, terminal, identification, and date code in accordance with MIL-STD-456. Terminal and part number identification shall be in accordance with figure 3. (See 4.5.2.1).

3.3.3 Workmanship. Workmanship shall be in accordance with MIL-STD-454, requirement 9. The multiplier shall be free from burrs, sharp edges, potting voids, defects and scratches which may affect performance. It shall also be free from grease, oil, dust, solder flux or any other conductive film. The process of fabrication and non-destructive testing shall not deteriorate the characteristics of multiplier performance material or appearance. (See 4.5.2).

3.3.4 Over voltage. There shall be no evidence of continuous arcing, or breakdown when the multiplier is subjected for 5 seconds to a voltage sufficient to cause 150% of rated output voltage to appear for a multiplier efficiency less than 88% and 130% of rated output voltage for a multiplier efficiency greater than 88%. (See 4.5.8).

3.3.5 Burn-in. All multipliers shall be burned in at no load of 48 hours at plus 52°C at 115% of rated output voltage for a multiplier efficiency greater than 88% and at 125% of rated output for a multiplier efficiency less than 88%. (See 4.3.1 and 4.4.1).

4. QUALITY ASSURANCE PROVISION.

4.1 Responsibility for Inspection.- Unless otherwise specified in the contract or purchase order the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may utilize his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government

reserves the right to perform any of the inspections set forth in the purchase description where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.2 Classification of inspection. The examination and testing of multipliers shall be classified as follows: (a) first article inspection (b) quality conformance inspection (does not include preparation for delivery).

4.3 First article inspection.

4.3.1 First article samples. When specified in the contract or purchase order the contractor shall furnish fifty(50) first article samples of each multiplier.

4.3.2 First article inspection. All multipliers shall be burned in in accordance with 3.3.5 prior to initiating the following inspections. Fifty units of each type shall be subjected to the inspections specified in Table 1 in the order shown. All sample units shall be subjected to the inspection of Group 1. Ten sample units shall be subjected to the inspection of Group II. Thirty-five (35) sample units shall be subjected to the inspections of Group III. The remaining five (5) sample units shall be subjected to the inspections of Group IV. No failures shall be permitted.

4.4 Quality Conformance Inspection.

4.4.1 Burn in. All multipliers shall be burned in in accordance with 3.3.5.

4.4.2 Group A Inspection.- Group A inspection shall consist of the examination and tests specified in Table II, in the order shown.

4.4.2.1 Sampling plan - Statistical sampling and inspection shall be in accordance with MIL-STD-105 for general inspection level II. the acceptable quality levels (AQL) shall be as specified in Table II. Major and minor defects shall be as defined in MIL-STD-105.

4.4.4.2 Rejected lots - If an inspection lot is rejected, the supplier may rework it to correct the defects, or screen out the defective units and resubmit for reinspection. Resubmitted lots shall be inspected using tightened inspection. Such lots shall be separate from new lots, and shall be clearly identified as reinspected lots.

4.4.3 Group B Inspection - Group B inspection shall consist of the tests specified in Table III in the order shown. They shall be performed on samole units that have been subjected to and have passed the group A tests unless it is more practical to select a separate sample from the lot for group B inspection.

4.4.3.1 Sampling plan - The sampling plan shall be in accordance with MIL-STD-105 for general inspection level II. The AQL shall be 1.0 percent defective.

4.4.3.2 Rejected lots - If an inspection lot is rejected, the supplier may rework it to correct the defects, or screen out the defective units, and resubmit for reinspection. Resubmitted lots shall be inspected using tightened inspection.

Such lots shall be separate from new lots, and shall be clearly identified as reinspected lots.

4.4.4 Group C Inspection. Group C inspection shall consist of the examination and tests specified in Table IV, in the order shown. Group C inspection shall be made on sample units selected from inspection lots which have passed the groups A and B inspections. Sample units shall be selected once a month. Five (5) sample units shall be selected for Subgroup 1. Five (5) sample units shall be selected and subjected to the inspections of Subgroup II. Sample units for Subgroup III testing shall be selected in accordance with paragraph 4.2.4 "Production Acceptance (Sampling) Phase of Production Reliability Tests" of MIL-STD-781. Three (3) sample units shall be selected and subjected to the inspections of Subgroup IV.

4.4.4.1 Disposition of sample units. Sample units which have been subjected to group C inspection shall be delivered on the contract or purchase order, if the lot is accepted and the sample units are still within specified electrical tolerance, and if the sample units are clean and smooth.

4.4.4.2 Noncompliance. If a sample fails to pass group C inspection the supplier shall take corrective action on the materials or processes, both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, processes, etc., and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the

Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the Government). Groups A and B inspections may be reinstituted; however, final acceptance shall be withheld until the group C re-inspection has shown that the corrective action was successful. In the event of failure after reinspection information concerning the failure and the corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

4.5 Methods of examination and test.

4.5.1 Inspection Conditions. Test will be conducted in accordance with the test procedures specified herein. Unless otherwise specified the following conditions shall apply.

a. Inspections and test shall be performed in accordance with the test conditions specified in the "GENERAL REQUIREMENTS" of MIL-STD-202.

b. Rated applied input voltage shall be 1000 volt ±1% peak to peak sine wave input.

c. Test frequency shall be within ±2% of the nominal value.

d. Nominal test frequency shall be 30 KHz.

e. No load output shall be less than 2 nanoamp.

f. Full load output shall be 500 ±50 nanoamps.

4.5.2 Visual and mechanical examination.

4.5.2.1 External. Multipliers shall be examined to verify that the materials, external design and construction, physical dimensions, weight, marking and workmanship are in accordance with the applicable requirements. (See 3.3.1.2, 3.2.2.4, 3.2.2.5, 3.3.2, 3.3.3).

4.5.2.2 Internal. Multipliers shall be disassembled and examined to verify that the materials, internal connections, lead wires, diodes capacitors, internal mounting, potting and workmanship are in accordance with the applicable requirements. (See 3.3.1, 3.3.1.7, 3.3.3).

4.5.3 Room temperature electrical performance.

4.5.3.1 Multiplier efficiency. With rated voltage applied, the multiplier output voltage shall be measured while the supply frequency is varied over the specified frequency ranges of 20 KHz to 40 KHz with the input voltage held constant. Measurements shall be performed at no load and full load. (See 3.2.1.1).

4.5.3.2 Input capacitance. The input capacitance for the multiplier shall be determined by a capacitance bridge or other suitable means at 500 volt peak to peak at 30 KHz using the circuit of figure 2. (See 3.2.1.2).

4.5.3.3 Charging current. the multiplier charging current shall be measured using the circuit of Figure 2. Measurements shall be made at no load at 20 KHz and 40 KHz at rated input voltage. (See 3.2.1.3).

4.5.3.4 Ripple voltage. The multiplier ripple voltage shall be measured using a Jennings Probe or other suitable device. Measurements shall be made with rated voltage applied at 30 KHz at full load of 500 nanoamps. (See 3.2.1.4).

4.5.4 Low temperature performance. the multiplier shall be maintained for a minimum of one hour at a temperature of minus 54°C prior to performance of the following tests. (See 3.2.4.2).

4.5.4.1 Multiplier efficiency. With rated voltage applied the multiplier output voltage shall be measured while the supply frequency is varied over the specified frequency range with the input voltage held constant. Measurements shall be performed at no load and full load. (See 3.2.4.2.1).

4.5.4.2 Input capacitance. The input capacitance for the multiplier shall be determined by a capacitance bridge or other suitable means at 500 volt peak to peak at 30 KHz using the circuit of figure 2. (See 3.2.4.2.2).

4.5.4.3 Charging current. The multiplier charging current shall be measured using the circuit of Figure 2. Measurements shall be made at no load at 20 KHz and 40 KHz at rated input voltage. (See 3.2.4.2.3).

4.5.4.4 Ripple Voltage. the multiplier ripple voltage shall be measured using a Jennings Probe or other suitable device. Measurements shall be made with rated voltage applied at 30 KHz at full load of 500 nanoamps. (See 3.2.4.2.4).

4.4.5 High temperature performance. The multiplier shall be maintained for a minimum of one hour at a temperature of plus 52°C prior to performance of the following tests. (See 3.2.4.1).

4.5.5.1 Multiplier efficiency. With rated voltage applied the multiplier output voltage shall be measured while the supply frequency is varied over the specified frequency range with the input voltage held constant. Measurements shall be performed at no load and full load. (See 3.2.4.1).

4.5.5.2 Input capacitance. The input capacitance for the multiplier shall be determined by a capacitance bridge or other suitable means at 500 volt peak to peak at 30 KHz using the circuit of figure 2. (See 3.2.4.1.2).

4.5.5.3 Charging current. The multiplier charging current shall be measured using the circuit of Figure 2. Measurements shall be made at no load at 20 KHz and 40 KHz at rated input voltage. (See 3.2.4.1.3).

4.5.5.4 Ripple voltage. The multiplier ripple voltage shall be measured using a Jennings Probe or other suitable device. Measurements shall be made with rated voltage applied at 30 KHz at full load of 500 nanoamps. (See 3.2.4.1.4).

4.5.6 Resistance to soldering heat. Multipliers shall be tested in accordance with method 210 of MIL-STD-202. the following details shall apply:

(a) Special preparation of specimen - Sample units shall not have been soldered during any of the previous tests.

(b) Depth of immersion in the molten solder - To a point 1/16 inch from the nearest insulating material.

(c) Test-condition 450 F ±10 F; immersion 3 seconds (see 3.2.2.1).

4.5.7 Terminal strength. Multipliers shall be tested for terminal secureness in accordance with method 211 of MIL-STD-202. The following details and exceptions shall apply:

(a) Test-condition letter - A.

(b) Applied force - Terminal secureness shall be tested by gradually applying a force of 1/4 pound to each pin terminal in the direction of the axis of the terminal. (See 3.2.2.3).

4.5.8 Over Voltage - A test voltage sufficient to achieve the required over voltage as specified in 3.3.4 shall be applied. The test potential shall be applied for 5 ±1/2 second. There shall be no load. During the test, multipliers shall be examined for evidence of continuous arcing, breakdown of insulations and abrupt changes in charging current. (See 3.3.4).

4.5.9 Solderability. Multipliers shall be tested in accordance with method 208 of MIL-STD-202. Each of the terminals is to be tested. (See 3.2.2.2).

4.5.10 Barometric pressure. Multipliers shall be tested as specified in 4.2.3.7 and in accordance with method 105 of MIL-STD-202. The following details and exception shall apply:

(a) input voltage shall be sufficient to cause 115% of rated output.

(b) Test-condition letter A. (See 3.2.4.3.7).

4.5.11 Mechanical vibration. The rated operating potential and loads shall be applied to the multiplier during vibration testing. The electrical test circuit shall be devised so that the multiplier can be monitored during test for evidence of arcing, breakdown or abrupt changes in charging current. (See 3.2.4.3.6).

4.5.11.1 Longitudinal vibration.- Rigidly mount the multiplier to the vibration table such that the radial axis of the curved multiplier is parallel to the direction of motion (for the rectangular multiplier the length axis is parallel to the direction of motion). Subject the multiplier to two (2) each thirty (30) minute sweeps over the frequency ranges of ten (10) Hertz to 3500 Hertz and back to ten (10) Hertz while maintaining a constant 2.5 g's for five (5) minutes at each of the frequencies 1020 Hz & 2080 Hz.

4.5.11.2 Transverse vibration. Rigidly mount the multiplier to the vibration table such that the radial axis of curved multiplier is perpendicular to the direction motion. (For the rectangular multiplier the length axis is perpendicular to the direction of motion). Subject the multiplier to two (2) each thirty (30) minute sweeps over the frequency range of ten (10) Hertz to 3500 Hertz and back to ten (10) Hertz while maintaining a constant 2.5 g's ±0,.2 acceleration. Subject

the multiplier to vibration of ten (10) g for five (5) minutes at each of the frequencies 1020 Hz, 2080 Hz, and 3140 Hz ±100 Hz.

4.5.12 Mechanical shock. The rated operating potential and loads shall be applied to the multiplier during shock testing. The electrical test circuit shall be devised so that the multiplier can be monitored during test for evidence of arcing, breakdown, or abrupt changes in charging current. Tests shall also be monitored with an accelerometer mounted on the test fixture near the multiplier. Pulse shape and amplitude shall be recorded. (See 3.2.4.3.5).

4.5.12.1 Longitudinal sawtooth. Rigidly mount the multiplier with the radial axis for the curved multiplier in a vertical plane, (longitudinal),(for the rectangular multiplier the length axis is mounted in a vertical plane) and subject the multiplier to five (5) shock pulses of nine (9) millisecond duration sawtooth wave form whose peak force is 140 g's ± 14 g's, as measured by a calibrated "Peak G" meter or oscilloscope. If there is no evidence of electrical or mechanical failure reverse the multiplier so that the shock is still parallel to the radial axis (length axis for the rectangular multiplier) and repeat the test.

4.5.12.2 Transverse sawtooth. Rigidly mount the multiplier such that the radial axis (length axis) for the rectangular multiplier is in a horizontal (transverse phase). With the multiplier thus mounted, subject the multiplier to ten (10) shock pulses with the direction of the force applied perpendicular to the radial axis (length axis for the rectangular

multiplier).

4.5.12 Longitudinal impulse. Mount the multiplier as in 4.2.3.12.1 and subject the multiplier to six (6) pulses of nominal half sine wave shape having a peak amplitude of not less than 500 g's and duration 0.10 ±0.05 milliseconds. Impact oscillations as measured by the monitoring accelerometer shall be less than 30 g's twelve (12) millisecond after initial pulse. Reverse the multiplier so that the pulse is still parallel to the radial axis (length axis for rectangular multiplier) but in the opposite direction, and subject it to five (5) pulses of nominal half sine wave shape having a peak amplitude of not less than 310 g's and duration of 0.10 ±0.05 milliseconds. Impact oscillations as measured by the monitoring accelerometer shall be less than 30 g's twelve (12) milliseconds after initial pulse. If there is no evidence of electrical or mechanical failure, continue the test.

4.5.13 Thermal Shock. Multipliers shall be tested in accordance with method 107D, of MIL-STD-202. Test condition B-1 shall apply. (See 3.2.4.3.1).

4.5.14 High Temperature Storage. Multipliers shall be subjected to a minimum storage period of 8 hours at plus 71°C. The ambient temperature shall then be gradually lowered to plus 52°C. Measurements shall be made of the multiplier efficiency and charging current in accordance with 4.5.5.1, and 4.5.5.3. (See 3.2.4.3.2).

4.5.15 Low Temperature Storage. Multipliers shall be subjected to a minimum storage period of 2 hours at minus 65°C. The ambient temperature shall then be gradually raised to minus 54°C. Measurements shall be made of the multiplier efficiency and charging current in accordance with 4.5.4.1 and 4.5.4.3 . (See 3.2.4.3.3).

4.5.16 Humidity Sealing. Multipliers shall be exposed to a relative humidity of not less than 95% at a temperature of plus 23°C. Time of exposure shall be six hours. Upon completion of the exposure time, the multiplier shall be tested with an overload voltage of 112 percent of rated ac voltage. The overload voltage shall be applied to the multiplier as soon as possible after removal from the humidity chamber and in no case shall this interval exceed six hours. The overload test shall be performed for a period of 48 hours. (See 3.2.4.3.4).

4.5.17 Reliability. Multipliers shall be life tested at 52 ± 5°C. Operation shall be continuous at full load of 500 nano amps. Applied input voltage shall correspond to the burn in voltage (3.3.5). At least once each week during operation, the multipliers shall be subjected to at least 10 discharges to ground through a 22 megohm resistor for a period not less than 8 seconds per discharge. The electrical test circuit shall be devised so that an open circuit or short circuit during full load operation can be detected and

the time of failure recorded. Measurements shall be made of the multiplier efficiency and no load charging current at least once each 200 hours of operating time. For pre-production qualification, accept/reject criteria shall be in accordance with MIL-STD-781, Test Plan IV, except that the total test time shall be in multiples of the specified MTTF of this specification. No replacement shall be allowed. For wuality conformance acceptance, accept/reject criteria shall be in accordance with MIL-STD-781, Test Plan V. Test time shall be in multiples of the specified MTTF and replacement shall be allowed.

5. PREPARATION FOR DELIVERY.

5.1 Packaging. Packaging of the multiplier shall be in accordance with the best commercial practice.

6. NOTES.

6.1 Intended use. the multiplier is intended for use in power supplies for second generation image intensifier tubes.

6.2 Ordering data. Procurement documents shall specify the following:

6.2.1 Specification. Title, number, revision, and date of this specification and any amendments thereto.

6.2.2. Packaging. Level of packaging and level of packing required for shipment.

6.2.3 First article. If first article samples are to be procured and the quantity if other than fifty (50).

6.2.4 <u>Quantity</u>. The quantity of multipliers to be supplied.

6.2.5 <u>Lot size</u>. The quantity of multipliers making up the lot size on which sampling is based if different from first article or quality conformance requirements.

6.3 <u>Definitions</u>:

6.3.1 <u>Multiplier efficiency</u>. Multiplier efficiency is defined as:

$$\frac{\text{Multiplier Output Voltage}}{\text{AC Input Voltage X No. Stages}}$$

6.3.2 <u>Rated Output voltage</u>. Rated output voltage for the multiplier is defined as: Multiplier efficiency x rated Ac input voltage x number of multiplier stages.

6.3.3 <u>Rated input voltage</u>. Rated input voltage is equal to 1000 VPP ±1%.

6.3.4 <u>Damage</u>. Damage is defined as any breakage, lossening, shift, deformation, failure of any finish, hardware, connection or component, increase or fluctuation in input current, corona, arcing, voltage instability, electrical failure of malfunctioning, or any deterioration quality, or failure to operate in accordance with the requirements of this specificiation.

TABLE 1

FIRST ARTICLE INSPECTION FOR ELECTRICAL AND ENVIRONMENTAL CHARACTERISTICS AND MECHANICAL DESIGN AND CONSTRUCTION

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH
Group I		
Visual and mechanical examination (external)	3.3.1.2 3.2.2.4, 3.2.2.5 3.3.2, 3.3.3	
Multiplier Efficiency	3.2.1.1, 3.2.4.1.1 3.2.4.2.1	4.5.3.1, 4.5.5.1 4.5.4.1
Charging Current	3.2.1.3, 3.2.4.1.3 3.2.4.2.3	4.5.3.3, 4.5.5.3 4.5.4.3
Input Capacitance	3.2.1.2, 3.2.4.1.2 3.2.4.2.2	4.5.3.2, 4.5.5.2 4.5.4.2
Group II		
Resistance to Soldering heat	3.2.2.1	4.5.6
Terminal Strength	3.2.2.3	4.5.7
Over Voltage	3.3.4	4.5.8
Solderability	3.2.2.2	4.5.9
Dielectric withstanding voltage at Barometric Pressure	3.2.4.3.7	4.5.10
Thermal Shock	3.2.4.3.1	4.5.13
High Temperature Storage	3.2.4.3.2	4.5.14
Low Temperature Storage	3.2.4.3.3	4.5.15
Humidity Sealing	3.2.4.3.4	4.5.16
Over Voltage	3.3.4	4.5.8
Multiplier Efficiency	3.2.1.1	4.5.3.1
Charging Current	3.2.1.3	4.5.3.3

FIRST ARTICLE INSPECTION CONTINUED

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH
Input Capacitance	3.2.1.2	4.5.3.2
Visual & Mechanical Examination (external)	3.3.2 3.3.3	4.5.2.1
Visual & Mechanical Examination (internal) (one sample unit)	3.3.1, 3.3.1.1 3.3.3	4.5.2.2
Group III		
Reliability	3.2.3	4.5.17
Over Voltage	3.3.4	4.5.8
Visual & Mechnaical	3.3.2 3.3.3	4.5.2.1
Multiplier Efficiency	3.2.1.1	4.5.3.1
Charging Current	3.2.1.3	4.5.3.3
Input Capacitance	3.2.1.2	4.5.3.2
Group IV		
Mechanical Vibration	3.2.4.3.6	4.5.11
Mechanical Shock	3.2.4.3.5	4.5.12
Over Voltage	3.3.4	4.5.8
Ripple Voltage	3.2.1.4 3.2.4.1.4, 3.2.4.2.4	4.5.3.4 4.5.5.4 4.5.4.4

TABLE II

GROUP A INSPECTION

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH	AQL (PERCENT DEFECTIVE) MAJOR	MINOR
Visual & Mechanical Examination (external)	3.3.1.2, 3.2.2.4 3.2.2.5, 3.3.2 3.3.3	4.5.2.1	0.65	4.0
Over Voltage	3.3.4	4.5.8	0.65	-
Multiplier Efficiency	3.2.1.1	4.5.3.1	0.65	-
Charging Current	3.2.1.3	4.5.3.3	0.65	-
Input Capacitance	3.2.1.2	4.5.3.2	0.65	-

TABLE III

GROUP B INSPECTION

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH
Multiplier Efficiency	3.2.4.1.1, 3.2.4.2.1	4.5.5.1, 4.5.4.1
Charging Current	3.2.4.1.3, 3.2.4.2.3	4.5.5.3, 4.5.4.3
Input Capacitance	3.2.4.1.2, 3.2.4.2.2	4.5.5.2, 4.5.4.2

TABLE IV

GROUP C INSPECTION

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH
Subgroup 1		
Thermal Shock	3.2.4.3.1	4.5.13
Over Voltage	3.3.4	4.5.8
High Temperature Storage	3.2.4.3.2	4.5.14
Low Temperature Storage	3.2.4.3.3	4.5.15
Subgroup 2		
Resistance to soldering heat	3.2.2.1	4.5.6
Terminal Strength	3.2.2.3	4.5.7
Humidity Sealing	3.2.4.3.4	4.5.16
Over Voltage	3.3.4	4.5.8
Reduced Barometric Pressure	3.2.4.3.7	4.5.10
Mechanical Vibration	3.2.4.3.6	4.5.11
Mechanical Shock	3.2.4.3.5	4.5.12
Over Voltage	3.3.4	4.5.8.7
Multiplier Efficiency	3.2.1.1	4.5.3.1
Charging Current	3.2.1.3	4.5.3.3
Input Capacitance	3.2.1.2	4.5.3.2
Visual & Mechanical Examination (external)	3.3.2 3.3.3	4.5.2.1
Visual & Mechanical Examination (internal, one sample)	3.3.1, 3.3.1.1 3.3.3	4.5.2.2

GROUP C INSPECTION CONTINUED

EXAMINATION OR TEST	REQUIREMENT PARAGRAPH	METHOD PARAGRAPH
Subgroup 3		
Reliability	3.2.3	4.5.17
Over Voltage	3.3.4	4.5.8
Visual & Mechanical Examination (external)	3.3.2, 3.3.3	4.5.2.1
Multiplier Efficiency	3.2.1.1	4.5.3.1.1
Charging Current	3.2.1.3	4.5.3.3
Input Capacitance	3.2.1.2	4.5.3.2
Subgroup 4		
Solderability	3.2.2.2	4.5.9
Ripple Voltage	3.2.1.4	4.5.3.4

"N" STAGE

MULTIPLIER MODULE CIRCUIT

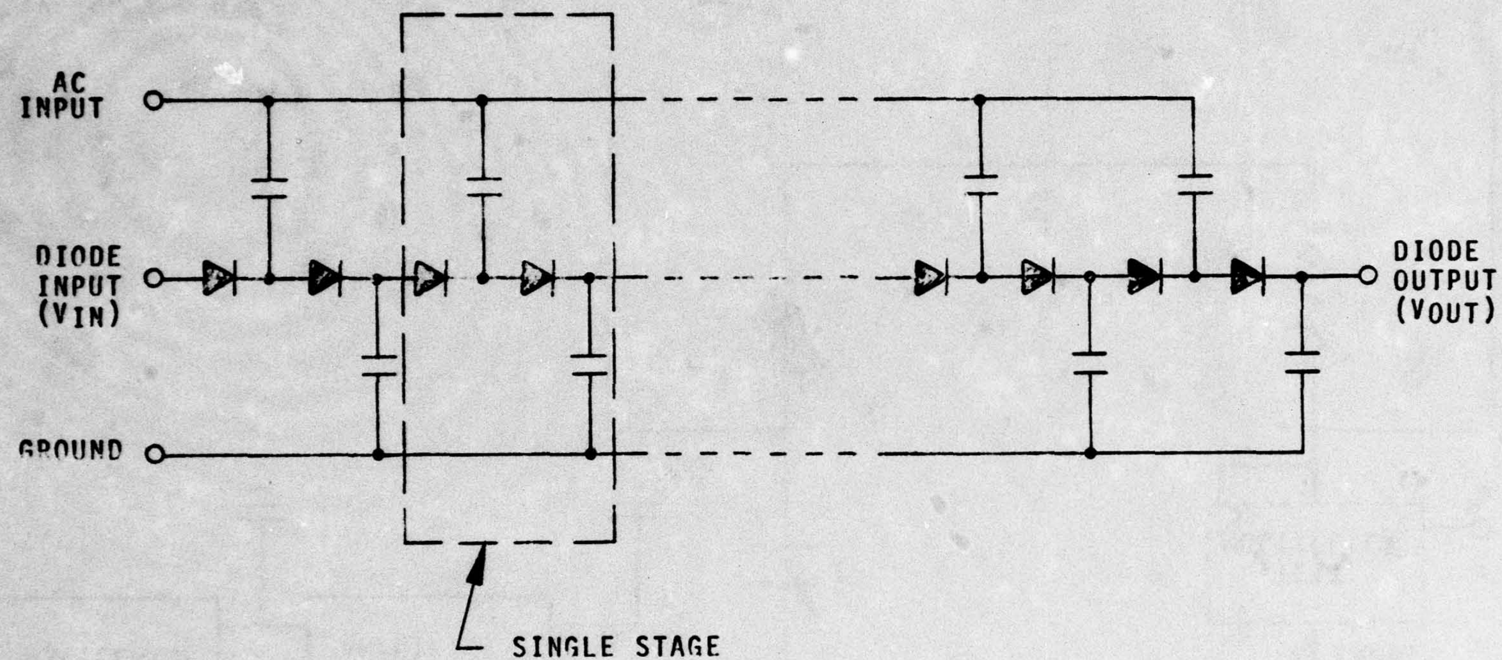
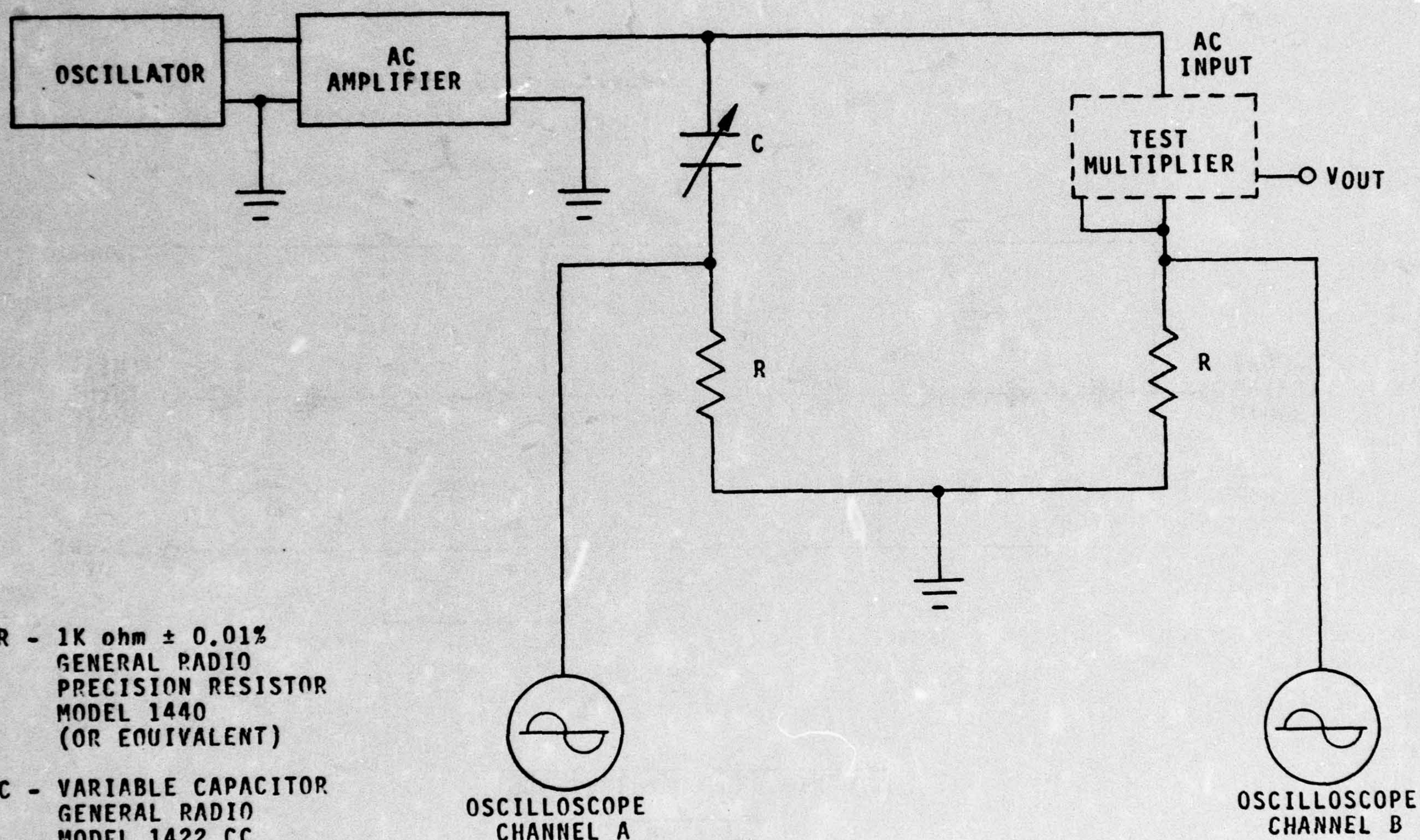


FIGURE 1

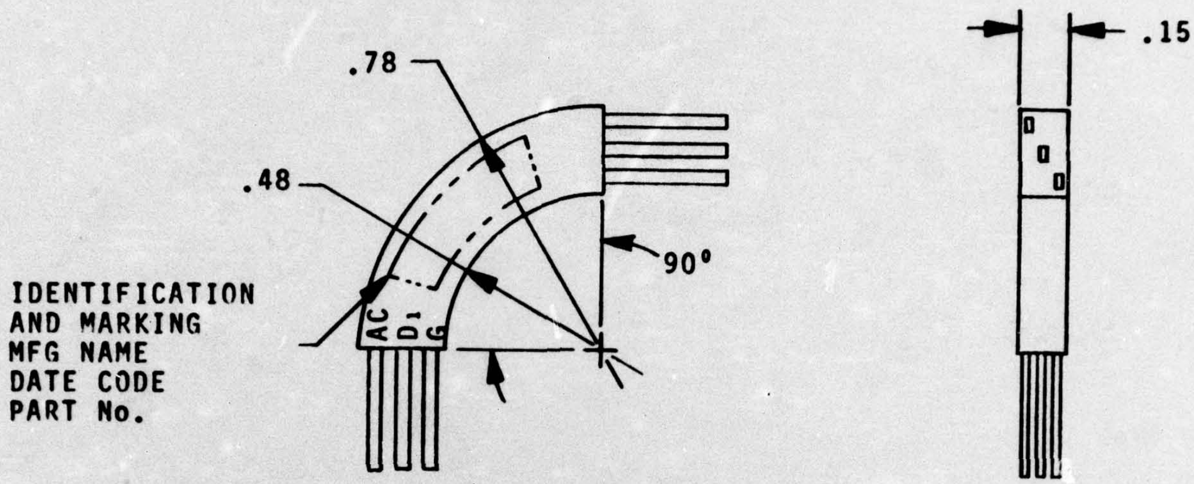
TEST CIRCUIT FOR INPUT CAPACITANCE AND CHARGING CURRENT



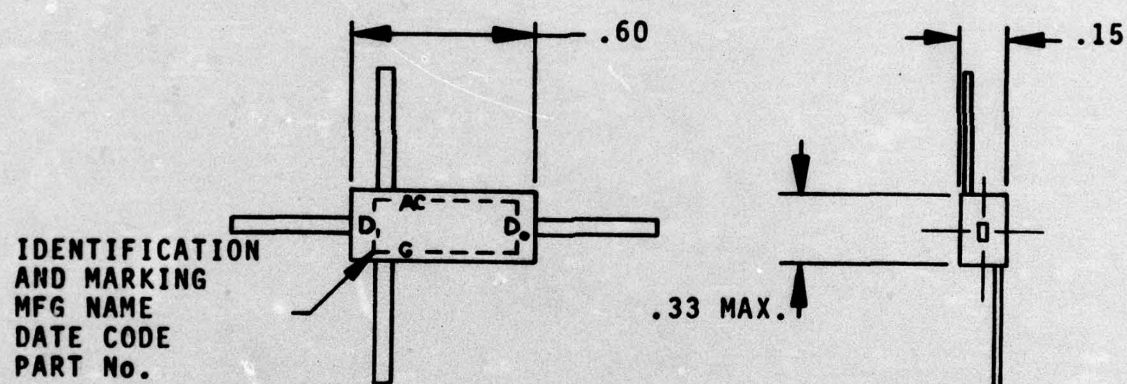
R - 1K ohm ± 0.01%
GENERAL RADIO
PRECISION RESISTOR
MODEL 1440
(OR EQUIVALENT)

C - VARIABLE CAPACITOR
GENERAL RADIO
MODEL 1422 CC
(OR EQUIVALENT)

FIGURE 2



6 STAGE CURVED MULTIPLIER MODULE



6 STAGE RECTANGULAR MULTIPLIER MODULE

NOTE:

1. TOLERANCES FOR ALL DIMENSIONS TO BE ESTABLISHED FOR OPTIMUM PRODUCTION REPRODUCIBILITY.

2. LEAD MATERIAL TO BE SELECTED FOR OPTIMUM PRODUCTION REPRODUCIBILITY.

FIG. 3. MULTIPLIER MODULES

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